

## CLAIMS:

1. A semiconductor device (100), in particular a S[ilicon]O[n]I[nsulator] device, comprising:
  - at least one isolating layer (10) made of a dielectric material;
  - at least one silicon substrate (20) arranged on said isolating layer (10);
  - 5 - at least one component (30) integrated in the silicon substrate (20), which component has at least one slightly doped zone (34); as well as
    - at least a first, in particular planar, metallization region (40) arranged between the isolating layer (10) and the component (30), in particular between the isolating layer (10) and the slightly doped zone (34) of the component (30), characterized in that at least a
    - 10 second, in particular planar, metallization region (42) is arranged on the side of the silicon substrate (20) facing away from the isolating layer (10), in the area of the component (30), particularly in the area of the slightly doped zone (34) of the component (30).
2. A semiconductor device as claimed in claim 1, characterized in that the silicon
- 15 substrate (20) comprising the component (30) is fixed onto the isolating layer (10) by means of at least one fixing medium (12), in particular by means of an adhesive layer.
3. A semiconductor device as claimed in claim 1 or 2, characterized in that
  - the component 30 is formed by at least one, particularly bipolar, pnp
  - 20 transistor; and
    - the slightly doped zone (34) of the component (30) is formed by the n-doped region of the pnp- transistor.
4. A semiconductor device as claimed in any one of the claims 1 through 3,
- 25 characterized in that the first metallization region (40) is embedded in at least a first, in particular oxide-based, passivation layer (22).

5. A semiconductor device as claimed in any one of the claims 1 through 4, characterized in that on the side of the component 30 facing the isolating layer 10, at least one oxide layer (24) borders on the component (30) and/or on the first passivation layer (22).
- 5 6. A semiconductor device as claimed in any one of the claims 1 through 5, characterized in that between the component (30) and the second metallization region (42) at least a second, in particular buried passivation layer (26), which is in particular oxide-based, is arranged.
- 10 7. A method of manufacturing at least one semiconductor device (100), in particular, as claimed in any one of the claims 1 through 6, wherein:
- at least one isolating layer (10) made of a dielectric material is provided with at least one silicon substrate (20) using, in particular, adhesive means;
  - at least one component (30) having at least one slightly doped zone (34) is

15 integrated in the silicon substrate (20); and

  - at least a first, in particular planar, metallization region (40) is arranged between the isolating layer (10) and the component (30), in particular between the isolating layer (10) and the slightly doped zone (34) of the component (30), characterized in that at

20 least a second, in particular planar, metallization region (42) is provided on the side of the silicon substrate (20) facing away from the isolating layer (10), in the area of the component (30), particularly in the area of the slightly doped zone (34) of the component (30).
8. A method as claimed in claim 7, characterized in that the first metallization region (40) is embedded in at least a first, in particular oxide-based passivation layer (22).
- 25 9. A method as claimed in claim 7 or 8, characterized in that at least a second, in particular buried, passivation layer (26), which is in particular oxide-based, is arranged between the component (30) and the second metallization region (42).
- 30 10. Application of at least a first, in particular planar, metallization region (40) as well as at least a second, in particular planar, metallization region (42) to electrically shield, on both sides, at least a component (30) incorporated in the silicon substrate (20) of a S[ilicon]O[n]I[n]sulator device (100) as claimed in any one of claims 1 through 6, in

particular to electrically shield, on both sides, at least a slightly doped zone (34) of the component (30).